IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1. (Currently amended) An apparatus comprising:

a circuit configured to receive an input clock signal and to generate an output phase synchronized to said input clock signal at a predetermined time delayed relative to said input clock signal, ~~and~~ wherein the predetermined time is dependent on a logic phase width of said input clock signal and on a ratio of capacitance values and is independent of at least one of the process parameters including transistor drive current, parasitic resistance, and parasitic capacitance.

2. (Original) The apparatus as in claim 1, wherein said predetermined time is relative to at least one of a rising edge of said input clock signal, and a failing edge of said input clock signal.

3. (Canceled)

4. (Original) The apparatus as in claim 1, wherein said circuit is further configured to provide a first signal and a second signal, compare said first signal and said second signal, and generate said output phase dependent on said comparison of said first signal and said second signal.

5. (Original) The apparatus as in claim 4, wherein said comparison is provided by a comparator.

6. (Original) The apparatus as in claim 1, wherein said apparatus is cascaded with at least one reproduction of said apparatus, and configured to provide a multiple of said input clock signal.

7. (Original) The apparatus as in claim 1, wherein said apparatus is coupled in parallel with at least one reproduction of said apparatus, and configured to provide at least two of said output phase generated in parallel during said input clock signal.

8. (Currently amended) A method comprising:

receiving an input clock signal and generating an output phase synchronized to said input clock signal at a predetermined time delayed relative to said input clock signal, ~~and~~ wherein the predetermined time is dependent on a logic phase width of said input clock signal and on a ratio of capacitance values and is independent of at least one of the process parameters including transistor drive current, parasitic resistance, and parasitic capacitance.

9. (Original) The method as in claim 8, wherein said predetermined time is relative to at least one of a rising edge of said input clock signal, and a falling edge of said input clock signal.

10. (Canceled)

11. (Original) The method as in claim 8, further comprising providing a first signal and a second signal, comparing said first signal and said second signal, and generating said output phase dependent on said comparison of said first signal and said second signal.

12. (Original) The method as in claim 8, further providing a multiple of said input clock signal.

13. (Canceled)

14. (Currently amended) A chipset comprising:

an embedded circuit block including a circuit configured to receive an input clock signal and to generate an output phase synchronized to said input clock signal at a predetermined time delayed relative to said input clock signal, ~~and~~ wherein the predetermined time is dependent on a logic phase width of said input clock signal and on a ratio of capacitance values and is independent of at least one of the process parameters including transistor drive current, parasitic resistance, and parasitic capacitance.

15. (Original) The chipset as in claim 14, wherein said predetermined time is relative to at least one of a rising edge of said input clock signal, and a falling edge of said input clock signal.

16. (Canceled)

17. (Original) The chipset as in claim 14, wherein said circuit is further configured to provide a first signal and a second signal, compare said first signal and said second signal, and generate said output phase dependent on said comparison of said first signal and said second signal.

18. (Original) The chipset as in claim 17, wherein said comparison is provided by a comparator.

19. (Original) The chipset as in claim 14, wherein said apparatus is cascaded with at least one reproduction of said apparatus, and configured to provide a multiple of said input clock signal.

20. (Original) The chipset as in claim 14, wherein said apparatus is coupled in parallel with at least one reproduction of said apparatus, and configured to provide at least two of said output phase generated in parallel during said input clock signal.

21. (Currently amended) A chipset comprising:

an embedded circuit block including means for receiving an input clock signal and generating an output phase synchronized to said input clock signal at a predetermined time delayed relative to said input clock signal, ~~and~~ wherein the predetermined time is dependent on a logic phase width of said input clock signal and on a ratio of capacitance values and is independent of at least one of the process parameters including transistor drive current, parasitic resistance, and parasitic capacitance.

22. (Original) The chipset as in claim 21, wherein said predetermined time is relative to at least one of a rising edge of said input clock signal, and a falling edge of said input clock signal.

23. (Canceled)

24. (Original) The chipset as in claim 21, wherein said embedded circuit block further comprising means for providing a first signal and a second signal, comparing said first signal and said second signal, and generating said output phase dependent on said comparison of said first signal and said second signal.

25. (Original) The chipset as in claim 21, said embedded circuit block further comprising means for providing a multiple of said input clock signal.

26. (Original) The chipset as in claim 21, said embedded circuit block further comprising means for providing at least two of said output phase generated in parallel during said input clock signal.